CLAIMS

Please amend the following claims.

1. (Three Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.

2. (Amended ) The transistor of Claim 1, further comprising a portion of the gate electrode that overlies the innermost portion of the source/drain extension.

3. (Amended) The transistor of Claim 2, wherein the gate electrode conforms to the recessed channel.

4. (Three Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, a portion of the gate dielectric layer overlaying an inner-most portion of the extension.

5. (Amended) The transistor of Claim 4, wherein a portion of the gate electrode overlies an innermost portion of the source/drain extension.

7. (Three Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a curvilinear shape;

a gate dielectric layer disposed superjacent the curvilinear recess;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess, a portion of the gate dielectric layer overlaying an inner-most portion of the extension.

8. (Amended) The transistor of Claim 7, wherein a portion of the gate electrode overlies an innermost portion of the source/drain extension.

9. (Amended) The transistor of Claim 7, wherein the gate electrode conforms to the recessed channel.